

Appl. No. 09/531,026
Amdt. dated May 12, 2005
Preliminary Amendment

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A computer-implemented method comprising the steps of:
 - executing a program on a high level simulator of a processor; thereafter
 - dividing the program into a plurality of independent code fragments such that a destination branch of an instruction in each code fragment falls within that code fragment; thereafter
 - establishing a plurality of checkpoints; wherein each of the plurality of checkpoints is established along ~~one of a beginning point or an ending point~~ of a different one of the code fragments; thereafter
 - saving state data at each of said checkpoints; wherein said state data comprises:
 - program counter contents of said processor;
 - register contents of said processor;
 - cache memory contents of said processor;
 - main memory contents of said processor; and
 - branch prediction contents of said processor; thereafter
 - executing instructions in said program on a plurality of low level simulators of said processor in parallel, starting each of said low level simulators at a corresponding checkpoint with corresponding state data associated with said corresponding checkpoint, wherein said executing instructions step further comprises the steps of:
 - loading each of said low level simulators with said program;
 - initializing each of said low level simulators at said corresponding checkpoint with said corresponding state data associated with said corresponding checkpoint; and
 - executing said program on said low level simulator up to a certain point in said program; and thereafter

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generating functional data to validate functionality of the processor.

2. (Currently amended) The computer-implemented method of claim 1 further comprising:

generating performance data to validate performance of the processor.

3. (Currently amended) The computer-implemented method of claim 1 wherein each code fragments has one of random lengths and determined length.

4. Canceled.

5. (Currently amended) The computer-implemented method of claim 1 wherein said processor is one of (a) a microprocessor, (b) a digital signal processor, (c) an input/output (I/O) controller, and (d) a network processor.

6. (Currently amended) The computer-implemented method of claim 1 wherein said high level simulator is one of (a) an instruction accurate simulator (IAS) of said processor and (b) a cycle accurate simulator (CAS) of said processor.

7. (Currently amended) The computer-implemented method of claim 1 wherein each of said low level simulators is a register transfer level (RTL) model of said processor, written as one of (a) a VHDL model of said processor and (b) a Verilog model of said processor.

8. Canceled.

9. (Currently amended) The computer-implemented method of claim [[8]] 1 wherein said certain point is one of (a) a next checkpoint immediately following said corresponding checkpoint, (b) a point in said program a random length after said corresponding checkpoint, and (c) a point in said program a determined length after said corresponding checkpoint.

10. Canceled.

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11. (Currently amended) A computer readable media having stored thereon a program comprising computer readable instructions for:

executing a program on a high level simulator of a processor; thereafter

dividing the program into a plurality of independent code fragments such that a destination branch of an instruction in each code fragment falls within that code fragment; .
thereafter

establishing a plurality of checkpoints; wherein each of the plurality of checkpoints is established along one of a beginning point or an ending point of a different one of the code fragments; thereafter

saving state data at each of said checkpoints; wherein said state data comprises:

program counter contents of said processor;

register contents of said processor;

cache memory contents of said processor;

main memory contents of said processor; and

branch prediction contents of said processor; thereafter

executing instructions in said program on a plurality of low level simulators of said processor in parallel, starting each of said low level simulators at a corresponding checkpoint with corresponding state data associated with said corresponding checkpoint; wherein said executing of instructions further comprises the steps of:

loading each of said low level simulators with said program;

initializing each of said low level simulators at said corresponding checkpoint with said corresponding state data associated with said corresponding checkpoint; and

executing said program on said low level simulator up to a certain point in said program; and thereafter

generating functional data to validate functionality of the processor.

12. (Currently amended) The computer readable media of claim 11 further comprising instructions for:

generating performance data to validate performance of the processor.

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13. (Previously presented) The computer readable media of claim 11 wherein each code fragments has one of random length and determined length.

14-15. Canceled.